MIPS64 5K™ LV (5Kc, LSS LJA0004) Specification Update

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1 Preface

This document communicates updates to the specifications of the family of MIPS32 4K™ and MIPS64 5K™ Processor Lead Vehicles contained in the document *MIPS 4K/5K™ Lead Vehicle datasheet*, Ref 1.

There are variations in the characteristics of the Lead Vehicles. These are due to the variations in the type, revision, and configuration of the Lead Vehicle, and they are dependent on the vendor, the process technology, and the production series. Through the on-going validation and characterization of the Lead Vehicles, MIPS identifies updates and additions to the information in the documentation for the Lead Vehicles. The Specification Updates in this document are specific to the

- *MIPS64 5Kc Processor Lead Vehicle with manufacturing ID LSS LJA0004*.

The Specification Updates can be classified as deviations from the generic specifications, additional information, or defects.

The document is primarily intended for hardware system developers building boards equipped with MIPS32 4K or MIPS64 5K Processor Lead Vehicles.

The document presents additional information and detailed descriptions of deviations from the specifications in the datasheet. There are sections for updates to the chip pin description, AC & DC specifications, power supply, operating frequency, and other specification updates.

A separate section describes the SW initiated configuration changes that is possible in the actual hardware configuration (see Table 2) of the MIPS 5Kc

Defects are listed in overview form in the errata information section. A detailed description of the defects are given in section 4. This includes description of the problem, the implication on the system, a suggested work around, and status. The status of an errata will be described by one of the following codes:

Table 1 Status Codes Used In Summary Tables

Code	Description
Open	This issue is under investigation.
Fix	This issue is intended to be fixed in a future version of the component.
Fixed	This issue has been fixed in a previous version.
NoFix	There are no plans to fix this issue.
Doc	The appropriate documents will be updated in the future.

1.1 Emphasis of Range Violations and Document Modifications

Throughout the document a shaded field in a table is used to emphasize that this value is deviating from, or violating, the range specified in the datasheet.

2 Specification Updates to LSS LJA0004

In this section specific information on this particular Lead Vehicle is provided. The information is structured as a set of sub-sections containing specifications that must be present for each Lead Vehicle. These sub-sections are a supplement to the datasheet and consist of

- Basic Information
- Errata Information
- Supply Voltages and Environmental Conditions
- Test-related Pin-out
- DC Specifications
- AC Specifications
- PLL Connections and Loop Filter

The remaining sections contains Specification Updates that are unique for this Lead Vehicle and thus not covered elsewhere.

2.1 Basic Information

The basic information for the Lead Vehicle is summarized in Table 2.

Table 2 Lead Vehicle Information

Parameter	Value
Vendor	LSS (MIPS Technologies)
Type	5Kc core
Part ID	LSS LJA0004
Data Cache	2-way, 4 kByte sets, 8kByte total, No Parity
Instruction Cache	2-way, 4 kByte sets, 8kByte total, No Parity
MMU	TLB with 32 dual entries
EJTAG Support	Version 2.5 4 I breaks, 2 D breaks, TAP module
RTL Version	1.3
Static Input Signals to Core:	
EJ_ManufID[10:0] EJ_PartNumber[15:0]	0x0 0x0
EJ_Version[3:0]	0x0
CP0 PRID Value	0x018101

2.2 Errata Information

Table 3 contains an overview of the present errata information on this LV implementation of the MIPS 5Kc. The listed errata information only concerns the LV implementation and not the MIPS 5Kc itself. For errata information on the latter see Ref 2. Section 4 contains a detailed description of the LV errata.

Table 3 Errata information

Errata#	Description
L1	The EJTAG Device ID Register does not contain the correct value.
L2	The on-chip PLL is not functional.

2.3 Supply Voltages and Environmental Conditions

The Lead Vehicle's three power supply voltages, the I/O power supply, the core power supply, and the PLL power supply (quiet Vss, Vdd) are listed in Table 4 together with the operating ambient temperature

Table 4 Supply Voltages and Operating Ambient Temperature

Parameter	Value	Tolerance
VDD (I/O buffers)	3.3 V	10 %
CVDD (Core supply)	2.5 V	8 %
VDDA (PLL supply)	2.5 V	8 %
Operating ambient temperature	0 ^{o}C to +70 ^{o}C	-

There are no special requirements to the order in which the power supplies are powering up, or down.

2.4 Test-related Pin-out

The following table lists deviations and additions to the functional pin descriptions given in the datasheet. Table 5 shows the format of the implementor test pins. The test pins are only for internal undocumented use. The input pins should be left de-asserted.

Table 5 Test Pin Description

Test mode pins (implementor use only)			
Pin name	**Type**	**Control Pin**	**Description**
TIN[0]	I		Not used
TIN[1]	I		Not used
TIN[2]	I		Not used
TIN[3]	I		Used as test clock input in LSS's proprietary "stuck at" production test
TIN_N[0]	I		Not used
TIN_N[1]	I		Not used
TIN_N[2]	I		Not used
TIN_N[3]	I		Not used

Table 5 Test Pin Description

Test mode pins (implementor use only)			
Pin name	**Type**	**Control Pin**	**Description**
TOUT[0]	O		Not used
TOUT[1]	O		Not used
TOUT[2]	O		Not used
TOUT[3]	O		Not used

2.5 DC Specifications

The I/O cells on this Lead Vehicle are all from the LVCMOS3 Interface family in the LSS ASIC cell library E4.

Table 6 Recommended Operating Condition

Parameter	Description	Min	Nom	Max
VDD	I/O buffer supply voltage	3.0 V	3.3 V	3.6 V
V_I	Input voltage	-0.5 V		5.5 V
V_O	Output voltage	0 V		VDD - 0.1 V
V_{IH}	High-level input voltage	2.0 V		5.5 V
V_{IL}	Low-level input voltage	-0.5 V		0.8 V

Table 7 Electrical Characteristics

Parameter	Condition	Min	Max
V_{OH}	I_O = rated	2.4V	
V_{OL}	I_O = rated		0.4
I_{IH}	$V_I = V_I$ max		+/- 10 µA
I_{IL}	$V_I = V_I$ max		+/- 10 µA
I_{OZ}	VDD = nominal V		+/- 100 µA

The input drivers are all of the same type, IFFPLDL, and the output drivers are of type O04LFF, T04LFF, B04LFFPLDL and B08LFFPLDL. Table 8 lists the capacitive loading for all used IO driver types. For the output drivers the rated I_O is included, as well. The capacitive loading (i.e. the capacitance on the input pins of the input drivers, and the capacitance on the output of the output driver) are the typical values for a nominal process under nominal conditions at VDD = 3.3 V.

Table 8 Driver Characteristics

Driver	I/O	Capacitive Load	I_O
IFFPLDL	I	5 pF	-
T04LFF	O	5 pF	4 mA
O04LFF	O	5 pF	4 mA
B04LFFPLDL	O	5 pF	4 mA
B08LFFPLDL	O	5 pF	8 mA

2.6 AC Specifications

This section shows any deviations of the AC specifications from the corresponding descriptions in the datasheet. First, an overview of the clock AC specifications is provided. Then, tables for the AC requirements of the pins are presented.

Due to the faulty PLL (see paragraph 2.2), the AC/DC pin specifications in SysAD64 mode (Table 11) is referenced to GCLKB. The LV is functional in PLL bypass mode (GBYPASS =1). In this mode the clock output GCLKB should be used as the source for any external SysAD agent.

2.6.1 Clock Signals

Table 9 shows the frequency and duty cycle ranges for all the input clock pins in the Lead Vehicle. The duty cycle is here specified as the percentage of the cycle where the phase is high. Due to the faulty PLL (see paragraph 2.2) all specification data with reference to the PLL has been omitted

The LSS LV has a non configurable clock multiplication factor of 2 (corresponding to GMULT[1:0]=1).

Table 9 Clocking Frequency and Duty Cycle Range

Pin, Mode	Min	Max
Core clock frequency range.	0 MHz	41.5 MHz
PLL output frequency range	PLL not functional	PLL not functional
GCLK frequency range, SysAD64 (PLL enabled), x2 mode => GMULT[1:0]=1	PLL not functional	PLL not functional
GCLK frequency range, SysAD64 (PLL enabled), x3 mode => GMULT[1:0]=2	PLL not functional	PLL not functional
GCLK frequency range, SysAD64 (PLL enabled), x3 mode => GMULT[1:0]=3	PLL not functional	PLL not functional
GCLK duty cycle, SysAD64 (PLL enabled)	PLL not functional	PLL not functional
GCLK frequency range, SysAD64 (PLL disabled)	0 MHz	41.5 MHz
GCLK duty cycle, SysAD64 (PLL disabled)	40	60
GCLK frequency range, core bond-out (PLL disabled)	0 MHz	41.5 MHz
GCLK duty cycle, core bond-out (PLL disabled)	40	60
ETCK frequency range	0 MHz	40 MHz
ETCK duty cycle	min. 10 ns high, and min. 10 ns low	

2.6.2 Other functional pins

The following three tables lists the AC/DC pin specifications.

Table 10 AC/DC Pin Specifications For Shared Function Pins

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GCLK	I	IFFPLDL						
GCLKB	O	O04LFF	25	CoreCLK	-1	1		
GRST2_N	I	IFFPLDL		DC				
GBYPASS	I	IFFPLDL		DC				
GMULT[1:0]	I	IFFPLDL		DC				
CBIGEN	I	IFFPLDL		DC				
CTIMER5	I	IFFPLDL		DC				
CSYSAD	I	IFFPLDL		DC				
CPIPEWR	I	IFFPLDL		DC				
C4WBLK	I	IFFPLDL		DC				
ETCK	I	IFFPLDL						
ETMS	I	IFFPLDL		DC				
ETDI	I	IFFPLDL		ETCK			10	0
ETDO	O (3S)	O04LFF	25	ETCK[a]	2	18		
ETRST_N	I	IFFPLDL		DC				
EDINT	I	IFFPLDL		ASYNC				
ERES[11:0]	O	O04LFF						
TSE	I	IFFPLDL		DC				
TSM	I	IFFPLDL		DC				
TSI	I	IFFPLDL		DC				
TSO	O	O04LFF	25		2	18		
TIN[3:0]	I	IFFPLDL		DC				
TIN_N[3:0]	I	IFFPLDL		DC				
TOUT[3:0]	O	O04LFF						
MBUS	I	IFFPLDL		DC				

Table 10 AC/DC Pin Specifications For Shared Function Pins

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
MINP[3:0]	I	IFFPLDL		DC				
MINP_N[3:0]	I	IFFPLDL		DC				

a. The ETDO output timing is specified relative to the negative edge of ETCK.

Table 11 AC/DC pin specs for SysAD64 mode

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GRST_N	I	IFFPLDL		ASYNC				
SSYSAD[63:0]	I/O	B08LFFPLDL	25	GCLKB	2	10	15	0
SSYSCMD[8:0]	I/O	B08LFFPLDL	25	GCLKB	2	10	15	0
SSYSADC[7:0]	I/O	B08LFFPLDL	25	GCLKB	2	10	15	0
SSYSCMDP	I/O	B08LFFPLDL	25	GCLKB	2	10	15	0
SRDRDY_N	I	IFFPLDL		GCLKB			15	0
SWRRDY_N	I	IFFPLDL		GCLKB			15	0
SVALIDIN_N	I	IFFPLDL		GCLKB			15	0
SVALIDOUT_N	O	O04LFF	25	GCLKB	2	10		
SEXTRQST_N	I	IFFPLDL		GCLKB			15	0
SRELEASE_N	O	O04LFF	25	GCLKB	2	10		
IINT_N[5:0]	I	IFFPLDL		ASYNC				
INMI_N	I	IFFPLDL		ASYNC				

Table 12 AC/DC pin specs for core bond-out mode

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_A[35:2]	O	O04LFF	25	GCLK	3	20		
EB_WData[63:0]	O	O04LFF	25	GCLK	3	20		
EB_RData[63:0]	I	IFFPLDL		GCLK			7	0
EB_BE[7:0]	O	O04LFF	25	GCLK	3	20		
EB_AValid	O	O04LFF	25	GCLK	3	20		

Table 12 AC/DC pin specs for core bond-out mode (Continued)

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_Write	O	O04LFF	25	GCLK	3	20		
EB_Instr	O	O04LFF	25	GCLK	3	20		
EB_Burst	O	O04LFF	25	GCLK	3	20		
EB_BFirst	O	O04LFF	25	GCLK	3	20		
EB_BLast	O	O04LFF	25	GCLK	3	20		
EB_BLen[1:0]	O	O04LFF	25	GCLK	3	20		
EB_ARdy	I	IFFPLDL		GCLK			7	0
EB_RdVal	I	IFFPLDL		GCLK			7	0
EB_WDRdy	I	IFFPLDL		GCLK			7	0
EB_RBErr	I	IFFPLDL		GCLK			7	0
EB_WBErr	I	IFFPLDL		GCLK			7	0
EB_WWBE	O	O04LFF	25	GCLK	3	20		
EB_EWBE	I	IFFPLDL		GCLK			7	0
EB_SBlock	I	IFFPLDL		GCLK			7	0
SI_Int[5:0]	I	IFFPLDL		GCLK			7	0
SI_NMI	I	IFFPLDL		GCLK			7	0
SI_ColdReset	I	IFFPLDL		GCLK			7	0
SI_Reset	I	IFFPLDL		GCLK			7	0
SI_MergeMode[1:0]	I	IFFPLDL		GCLK			7	0
SI_RP	O	O04LFF	25	GCLK	3	20		
SI_Sleep	O	O04LFF	25	GCLK	3	26		
SI_TimerInt	O	O04LFF	25	GCLK	3	23		
SI_ERL	O	O04LFF	25	GCLK	3	20		
SI_EXL	O	O04LFF	25	GCLK	3	20		
EJ_PerRst	O	O04LFF	25	GCLK	3	20		
EJ_PrRst	O	O04LFF	25	GCLK	3	20		
EJ_SRstE	O	O04LFF	25	GCLK	3	20		
EJ_DebugM	O	O04LFF	25	GCLK	3	20		

Table 12 AC/DC pin specs for core bond-out mode (Continued)

Pin name	Type	Buffer Type	External load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
PM_DCacheHit	O	O04LFF	25	GCLK	3	20		
PM_DCacheMiss	O	O04LFF	25	GCLK	3	20		
PM_ICacheHit	O	O04LFF	25	GCLK	3	20		
PM_ICacheMiss	O	O04LFF	25	GCLK	3	20		
PM_InstnComplete	O	O04LFF	25	GCLK	3	20		
PM_ITLBHit	O	O04LFF	25	GCLK	3	20		
PM_ITLBMiss	O	O04LFF	25	GCLK	3	20		
PM_JTLBHit	O	O04LFF	25	GCLK	3	20		
PM_JTLBMiss	O	O04LFF	25	GCLK	3	20		
PM_WTBMerge	O	O04LFF	25	GCLK	3	20		
PM_WTBNoMerge	O	O04LFF	25	GCLK	3	20		
PM_DTLBHit	O	O04LFF	25	GCLK	3	20		
PM_DTLBMiss	O	O04LFF	25	GCLK	3	20		

2.7 PLL Connections and Loop Filter

Table 13 shows the pin-out for the 6 analog connections to the PLL (quiet supplies, optional loop filter etc.).

Table 13 PLL Pin-Out

B13	D13	A13	C14	B12	C13
NC	NC	VSSA	NC	VDDA	NC

The LSS Lead Vehicle uses an internal loop filter.

3 Software-configurable Features of the 5K core in the Lead Vehicle

This Lead Vehicle allows the manipulation of some otherwise read-only bits in the CP0 Config register. The features that can be modified are the cache configuration bits in the Config Select 1 Register. The ability to change these features in software enables evaluation and benchmarking of the effect of different caches sizes and organizations beyond the default cache implemented on this Lead Vehicle.

The features described in this section are present specifically to support configuration testing of the core in a Lead Vehicle, and are not supported in any other environment. Attempting to use these features outside of the scope of a Lead Vehicle is a violation of the MIPS Architecture, and may cause unpredictable operation of the processor.

3.1 Config Register Format — Select 0

Table 14 Config Register Format-Select 0

31	30 28	27 25	24 21	20	19	18 17	16	15	14 13	12 10	9 7	6 3	2 0
M	K23	KU	0	ISD	WC	0	BM	BE	AT	AR	MT	0	K0

The format of Config (Select 0) Register is shown in Table 14 and the bit fields are described in Table 15 Most of the fields are identical to the description of this register in the *MIPS64 5K™ Processor Core Family Software User's Manual*, but the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- WC (bit 19): This bit is a write enable for the software-configurable features within the Config Register available on this Lead Vehicle. It can be written to either 1 or 0, but is initialized to 0. When this field is set to 1, the cache configuration fields in Config Select 1 become writeable.

Table 15 Config Register Field Descriptions

Fields		Description	Read/Write	Reset State
Name	Bit(s)			
M	31	This bit is hardwired to '1' to indicate the presence of the Config register.	R	1
K23	30:28	Specifies the kseg2 and kseg3 cache coherency algorithm to be used with an FMT-based MMU. Refer to Table 16 for the encoding of this field.	R/W	Undefined
KU	27:25	Specifies useg/kuseg cache coherency algorithm to be used with an FMT-based MMU. Refer to Table 5-6 for the encoding of this field. Refer to Table 16 for the encoding of this field.	R/W	Undefined
0	24:21	Reserved. Must be written as zero; returns zero on read	R	0
ISD	20	Instruction Scheduling Disable. Disable the instruction scheduling feature of the processor. 0: Instruction Scheduling enabled 1: Instruction Scheduling disabled	R/W	0
WC	19	Write Control. Enable write control of cache size and special function bits in the Config1 register. 0: Write control disabled 1: Write control enabled	R/W	0
0	18:17	Reserved. Must be written as zero; returns zero on read	R	0

Table 15 Config Register Field Descriptions (Continued)

Fields		Description	Read/Write	Reset State
Name	Bit(s)			
BM	16	Burst Mode. Selects between incremental and interleaved bus burst ordering. 0: Incremental 1: Interleaved	R	Preset or Externally Set
BE	15	Indicates the current endian byte-ordering convention. 0: Little endian 1: Big endian	R	Preset or Externally Set
AT	14:13	Architecture Type. Indicates the architecture type implemented by the processor. 1: MIPS64 with 32-bit address only 2: MIPS64 with 32/64-bit addresses The value 1 is used when the MMU type is FMT and the value 2 is used when the MMU type is TLB.	R	2
AR	12:10	Architecture Revision. Specifies the architecture revision level. 0: Revision 1	R	0
MT	9:7	MMU Type. Specifies the type of MMU implemented. 1: Standard TLB 3: Standard FMT	R/W	1
0	6:3	Reserved. Must be written as zero; returns zero on read	R	0
K0	2:0	Specifies the kseg0 cache coherency algorithm. Refer to Table 16 for the encoding of this field.	R/W	2

Table 16 Cache Coherency Attributes

C Value	Cache Coherency Attribute
0	Cacheable, noncoherent, write through, no write-allocate
1	Cacheable, noncoherent, write through, write-allocate
2	Uncached (write-arround)
3-6	Cacheable, noncoherent, write-back (write-allocate)
7	Uncached accelerated

3.2 Config1 Register Format — Select 1

Table 17 Config Register Format-Select 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MMU Size						IS			IL			IA			DS			DL			DA			0			PC	WR	CA	EP	FP

The format of Config (Select 1) Register is shown in Table 17 and the bit fields are described in Table 18 Most of the fields are identical to the description of this register in the *MIPS64 5K™ Processor Core Family Software User's Manual* but the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- The instruction cache configuration fields (IS, IL and IA) and the data cache configuration fields (DS, DL and DA) which are otherwise read-only become writeable when the WC bit in the Config Select 0 register is set. Note that only certain values for these fields are legal, while other encodings are reserved.

Table 18 Config1 Register Field Descriptions — Select 1

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
0	31	Reserved. Must be written as zero; returns zero on read	R	0
MMU Size	30:25	Number of entries in the TLB minus one. This field can have the following values: 0: Value used when the MMU is not TLB-based 15: 16-entry TLB MMU (dual entries) 31: 32-entry TLB MMU (dual entries) All other values are reserved.	R	31
IS	24:22	This field contains the number of instruction cache sets per way. No options are available. All other values are reserved. 1: 128 sets All other values are reserved.	R/W	128
IL	21:19	This field contains the instruction cache line size. I-cache line size. 0: No I-cache present 4: 32 bytes All other values are reserved.	R/W	4
IA	18:16	This field contains the level of instruction cache associativity. 0x0: Direct mapped 0x1: 2-way 0x2 - 0x7: Reserved	R/W	1
DS	15:13	This field contains the number of data cache sets per way. No options are available. All other values are reserved. 1: 128 sets All other values are reserved.	R/W	128

Table 18 Config1 Register Field Descriptions — Select 1 (Continued)

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
DL	12:10	This field contains the data cache line size. D-cache line size. 0: No D-cache present 4: 32 bytes All other values are reserved.	R/W	4
DA	9:7	This field contains the level of data cache associativity. 0x0: Direct mapped 0x1: 2-way 0x2 - 0x7: Reserved	R/W	1
0	6:5	Reserved. Must be written as zero; returns zero on read	0	0
PC	4	Performance Counter. This bit is 1 to indicate that the processor implements Performance Counter registers. 0: No performance counter registers implemented 1: At least one performance counter register implemented	R	1
WR	3	Watch registers implemented. 0: No watch registers implemented 1: At least one watch register implemented	R	1
CA	2	Code compression (MIPS16™ ASE) implemented. 0: No code compression 1: Code compression	R	0
EP	1	EJTAG implemented. 0: No EJTAG implemented 1: EJTAG implemented	R	1
FP	0	FPU implemented. 0: No FPU 1: FPU implemented	R	0

3.3 Cache configuration in Config Select 1

The cache configuration bits in the Config Select 1 Register can be written to modify the default cache size and organization.

Here is the sequence which must be used to accomplish a change in the cache configuration bits. This sequence should be executed in uncacheable space to avoid unpredictable behavior.

1. MTC0 instruction to set WC field in Config Select 0.
2. One or more additional MTC0 instructions to write the instruction and data cache configuration bits in Config Select 1 to their desired values.

Here are some additional considerations to keep in mind:

- Obviously, you cannot select a larger cache size or organization than the largest size present on the 5K core in the Lead Vehicle.
- The instruction and data caches can be configured independently.
- It is possible to disable a cache by setting the line size field (IL or DL) to zero.
- Only certain values for the cache configuration fields are legal in the 5K processor core, as detailed in Table 18.
- If you downsize or disable a cache with this method, only new line allocations are disabled. Loads or stores to “old” entries will still hit, even if they are in that part of the cache which has been downsized. If you do not desire this behavior, then you should initialize all the tag entries for the maximum cache configuration to be invalid before you select your new cache configuration.

4 LV Errata

L1. The EJTAG Device ID Register does not contain the correct value

Problem:

The ManufID and PartNumber fields in the EJTAG Device ID Register contains the wrong value. See Table 19

Table 19 EJTAG register contents

Register name	Register contents	
	Actual value	Correct value
EJ_ManufID[10:0]	0x0	0x127
EJ_PartNumber[15:0]	0x0	0x300

Implication:

The device will not be identified correctly and devices from other vendors might containing colliding values.

Work around:

None.

Status:

Fix (if a new version is made).

L2. The on-chip PLL is not functional

Problem:

The LV contains four on chip PLL's of which only one is used in the design. The PLL's are power supplied individually on four different die pads. The PLL that is being powered is by mistake of LSS not the used one.
The PLL is applied for clock doubling and phase alignment.

Implication:

The LV will not run in PLL mode.

Work around:

The LV is functional in PLL bypass mode (GBYPASS =1) using the clock output GCLKB as the source for the external SysAD agent. Note that the VDDA pin on the LV (B12) should be supplied with the required supply voltage even though the PLL is not used.

Status:

Fix (if a new version is made).

5 References

1. MIPS 4K/5K™ Lead Vehicle Datasheet
   Document no: MD00001
   MIPS Technologies, Inc.

2. MIPS64 5K™ Processor Core Family RTL Errata Sheet
   Document no: MD00031
   MIPS Technologies, Inc.

6 Revision history

Rev. Number	Date	Comments
01.00	Nov. 28, 2000	Initial Release.
01.01	Dec. 20, 2000	Updated after review
01.02	Dec. 29, 2000	Updated after 2nd review
01.03	July. 27, 2001	Updated after review of MD00140
01.04	Dec. 13, 2001	EJ_Version value changed to 0x0